



FORM HD-1449 (Based on Form PTO-1449)

PATENT AND TRADEMARK OFFICE
INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Sheet 1 of 4

ATTORNEY DOCKET NO.

MP0088

SERIAL NO.

09/920,241

APPLICANT

Pierte ROO

FILING DATE

August 1, 2001

GROUP

2631

U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.	81	6,201,841	03/2001	Iwamatsu et al.	—	
2.	81	6,576,746 B2	06/2003	McBride et al.	—	
3.	81	6,744,931	06/2004	Komiya et al.	—	

FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation Yes	No
1.		NONE					

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.	81	Rao, Sailesh; Short Course: Local Area Networks, International Solid State Circuits Conference; Sailesh Rao; Outline Implementing Gigabit Ethernet Over Cat-5 Twisted-Pair Cabling; Jack Kenny; Signal Processing and Detection in Gigabit Ethernet; Feb. 1999; 3 pages
2.	81	Techdictionary.com definition of decoder, Link: http://www.techdictionary.com ; Dec. 2005; 1 page
3.	81	University of Pennsylvania CSE Digital Logic Lab re decoders. Link: http://www.cse.dmu.ac.uk/~sexton/WWW/Pages/cs2.html ; Dec. 2005; 3 pages
4.	81	Maneatis, John G.; "FA 8.1: Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques; Nov. 1996; pp.1723-1732
5.	81	Dehng et al; "A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm"; IEEE Journal of Solid State Circuits, Vol. 36, No. 10; Oct. 2001; pp. 1464-1471
6.	81	Razavi; "Principles of Data Conversion System Design"; Textbook IEEE Press; Jan. 1995; 139 pages
7.	81	Mano; "Digital Logic and Computer Design"; Prentice Hall; copyright Jan. 1979; 627 pgs.

Examiner:


Date Considered:

12/18/07

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM HDP-1449 (Based on Form PTO-1449) PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION (Use several sheets if necessary) Sheet 2 of 4	ATTORNEY DOCKET NO.	SERIAL NO.
	MP0088	09/920,241
	APPLICANT	
	Pierte ROO	
	FILING DATE	GROUP
	August 1, 2001	2631

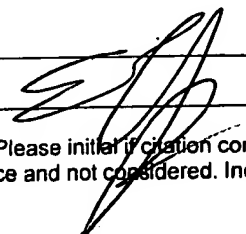
OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)		
Ref. Desig.	Examiner's Initials	
8.	ef	Farjad-rad, et al; "4.5 A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly Integrated Data Communication Chip"; 2002; 8 pgs. IEEE - ISSCC - Jan. 2000
9.	ef	Gotoh et al; "All-Digital Multi-Phase Delay Locked Loop for Internal Timing Generation in Embedded and/or High-Speed DRAMS"; IEEE Symposium on VLSI Circuits, Feb. 1997
10.	ef	Johnson et al; "THAM 11.2: A Variable Delay Line Phase Locked Loop for CPU-Coprocessor Synchronization"; IEEE Solid State Circuits Conf., Feb. 1988; pp. 142-143; 334-335.
11.	ef	Sonntag et al; "FAM: 11.5: A Monolithic CMOS 10MHz DPLL for Burse-Mode"; IEEE Solid State Circuits Conf.; Feb. 1990
12.	ef	Garlepp et al; "A Portable Digital DLL Architecture for CMOS Interface Circuits", Feb. 1998 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 214-215
13.	ef	Lin et al; "A Register-Controller Symmetrical DLL for Double-Data-Rate DRAM"; IEEE Journal Solid State Circuits; April 1999; pp. 565-568
14.	ef	Dehng et al; "Clock-Deskaw Buffer Using a SAR-Controlled Delay-Locked Loop"; IEEE Journal of Solid State Circuits; Nov. 2002; Vol. 35, No. 8; pp.1128-1136.
15.	ef	Kim et al; "A Low-Power Small-Area 7.28-ps-Jitter 1-GHz DLL-Based Clock Generator"; IEEE Journal of Solid State Circuits; Nov. 2002; Vol. 37, No. 11; Pgs. 1414-1420
16.	ef	Lin et al; "A 10-b, 500-Msample/s CMOS DAC in 0.6mm ² "; IEEE; Dec. 1996; 11 pgs.
17.	ef	Gray et al; "Analysis and Design of Analog Integrated Circuits", 04/09/2001; pp. 217-221.
18.	ef	Gray et al; "Analysis and Design of Analog Integrated Circuits", 04/09/2001; pp. 270 and 274
19.	ef	Dally et al; "Digital Systems Engineering"; Cambridge Univ. Press; June 1998; cover and pgs. 390-391
20.	ef	Hellwarth et al; "Digital-to-analog Converter having Common-mode Isolation and Differential Output"; IBM Journal of Research & Development; Jan. 1973
21.	ef	Shoval et al; "WA 18.7 - A Combined 10/125 Mbaud Twisted-Pair Line Driver with Programmable Performance/Power Features"; IEEE Int'l. Solid State Circuit Conf. Feb. 2000; Solid State Circuits, IEEE Journal of, Vol. 35, Issue 12, Nov. 2000; pp. 314-315
22.	ef	Chien; "Monolithic CMOS Frequency Synthesizer for Cellular Applications"; Solid State Circuits, IEEE Journal of, Vol. 35, Issue 12, Dec. 2000

Examiner: 	Date Considered: 12/18/07
---	---------------------------

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM HDP-1449 (Based on Form PTO-1449) PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION (Use several sheets if necessary) Sheet 3 of 4	ATTORNEY DOCKET NO.	SERIAL NO.
	MP0088	09/920,241
	APPLICANT	
	Pierte ROO	
	FILING DATE	GROUP
	August 1, 2001	2631

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)		
Ref. Desig.	Examiner's Initials	
23.	9	Chien; "Low-Noise Local Oscillator Design Techniques using DLL-based Frequency Multiplier for Wireless Applications"; Dissertation; Univ. of Calif., Berkley; Spring 2000
24.	el	Song; "Dual Mode Transmitter with Adaptively Controlled Slew Rate and Impedance Supporting Wide Range Data Rates"; ASIC/SOC Conf., Sept. 9-12, 2001
25.	9	Heliums et al; "An ADSL Integrated Active Hybrid Circuit"; Aug. 7, 2002
26.	el	He et al; "A DSP Receiver for 1000 Base-T PHY"; IEE Solid State Circuits Conf. 2001, Digest of Tech Papers; IEEE Journal of Solid State Circuits, Feb. 2001
27.	el	Roo et al; "A CMOS Transceiver Analog Front-end for Gigabit Ethernet over Cat-5 Cables"; Solid State Circuits Conf., Feb. 5, 2001, Digest of Technical Papers; Journal of IEEE Solid State Circuits, Feb. 2001
28.	9	Shoael et al; "A 3V Low Power 0.25µm CMOS 100Mb/s Receiver for Fast Ethernet"; May 6, 2001
29.	9	Chien et al; "TP 12.4: A 900-MHz Local Oscillator using a DLL-based Frequency Multiplier Technique for PCS Applications"; Journal of IEEE Solid State Circuits; Feb. 2000; pgs. 202-203 and 458
30.	9	Van de Plassche; "Integrated Analog-to-Digital and Digital-to-Analog Converters - Chapter 6"; Boston: Clower Academic Publishers; May 1994; pp. 211-271
31.	9	Millman et al; "Pulse, Digital, and Switching Waveforms"; June 1965; pp. 674-675
32.	9	Weigandt et al; "Analysis of Timing Jitters in CMOS Ring Oscillators"; IEEE Symposium on Circuits and Systems; May 1994; pp. 27-30
33.	el	Dally et al; "High Performance Electrical Signaling"; June 1998
34.	el	Munshi et al; "Adaptive Impedance Matching"; Dec. 1999; pp. 69-72
35.	el	Kim et al; "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design"; 1994 IEEE Symposium on Circuits and Systems; May 1994; pp. 31-34
36.	el	Lin et al; "TP 12.5: A 1.4 GHz Differential Low-Noise CMOS Frequency Synthesizer using a Wideband PLL Architecture"; Feb. 2000; pp. 204-205 and 458
37.	el	The Authoritative Dictionary of IEEE Standards Terms, 7th Edition; July 2000; page 280
38.	el	Goldberg, Lee; "Gigabit Ethernet PHY Chip Sets LAN Speed Record for CopperStory"; Tech Insights; Nov. 16, 1998

Examiner: 	Date Considered: 12/18/07
---	---------------------------

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM HDP-1449 (Based on Form PTO-1449) PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION (Use several sheets if necessary) Sheet 4 of 4	ATTORNEY DOCKET No.	SERIAL No.
	MP0088	09/920,241
	APPLICANT	
	Pierte ROO	
	FILING DATE	GROUP
	August 1, 2001	2631

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)		
Ref. Desig.	Examiner's Initials	
39.		Kelly, N. Patrick et al; "WA 18.5 - A Mixed-Signal DFE/FFE Receiver for 100Base-TX Applications", ISSCC 2000/Session 18/Wireline Communications/Paper WA 18.5, 2000 IEEE Int'l. Solid-State Circuits Conf., Feb. 7, 2000; pp. 310-311.
40.		Linear Technology, "High Speed Modem Solutions", InfoCard 20, Linear Technology Corporation, Dec. 1994
41.		Linear Technology, LT1355/LT1356, Dual and Quad 12MHz, 400V/us Op Amps, Linear Technology Corporation, Dec. 1994, pp. 1-16
42.		Linear Technology, LT1358/LT1359, Dual and Quad 25MHz, 600V/us Op Amps, Linear Technology Corporation, Dec. 1994, pp. 1-12
43.		Linear Technology, LT1361/LT1362, Dual and Quad 50MHz, 800V/us Op Amps, Linear Technology Corporation, Dec. 1994, pp. 1-12
44.		Linear Technology, LT1364/LT1365, Dual and Quad 70MHz, 1000V/us Op Amps, Linear Technology Corporation, Dec. 1994, pp. 1-12
45.		Linear Technology, LT1813/LT1814, Dual and Quad 3mA, 100MHz, 750V/us Op Amps, Linear Technology Corporation, Dec. 1994, pp. 1-16
46.		Yamaguchi et al; "400Mbit/s Submarine Optical Repeater Using Integrated Circuits", Fujitsu Laboratories Ltd.; Jan. 1986 (and English Language Translation)
47.		Uda et al; "125Mbit/s Fiber Optic Transmitter/Receiver with Duplex Connector", Fiber Optic Communications Development Div., NEC Corporation, NEC Engineering, Ltd., Fiber and Integrated Optics, Vol. 5, Issue 3; Jan. 1985 (and English Language Translation)
48.		IEEE Standards 802.3ab-2002, "Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications"; March 8, 2002; pp. 147-249

Examiner:	Date Considered: 12/18/07
-----------	---------------------------

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.